REMARKS

The Detailed Action mailed March 22, 2005 stated the following:

"This application contains claims directed to the following patentably distinct species of the claimed invention: species I: page 13 of specification, species II: page 35 of specification, and species III: page 37 of specification."

Species I (Page 13): On page 13, the applicant discloses a novel Gated-FET device as shown in Fig-4 of the application. This generic Gated-FET device is described in page 14-28, and shown to differ from MOSFET, JFET and SOI MOSFET devices from prior art as stated in page-14. In the prior art, the MOSFET and JFET devices are constructed as complementary pairs, (NMOS, PMOS) and (NFET, PFET) respectively, due to the complementing nature between -ve and +ve conductivity types. Similarly, the generic Gated-FET in this disclosure is also presented in a complimentary embodiment pair Gated-PFET and Gated-NFET as described in pages 15-19 (Figs. 5-8) and pages 19-23 (Figs. 9-12) respectively.

While the generic Gated-FET device comprises two distinct methods of construction embodiments, the operation and optimization is described in a single set of terms as shown in pages 24-28 via one set of parameters given in Eqs. 1-17. This is the case for NMOS & PMOS devices in prior art MOSFET devices as well, and can be seen in any text book related to semiconductor devices. Furthermore, a Gated-FET device also comprises an off-state, and an on-state similar to MOSFET or JFET devices. The off-state is described in pages 24-25 (Eqs. 1-8), while the on-state is described in pages 26-28 (Eqs. 9-17). Diagrammatically the results of the disclosed operation can be shown in both of the Gated-PFET and Gated-NFET embodiments, as the applicant has done in the disclosure.

In the Application, the applicant has also provided manufacturing methods to fabricate the Gated-FET device. These processing steps are detailed in pages 28-39 with respect to Figs. 13-14. A detailed Gated-FET fabrication using semiconductor materials is disclosed in pages 29-31. A plurality of process sequences may be employed to fabricate the Gated-FET device, and two possible embodiments are illustrated in the Application. A first process sequence is disclosed in pages 33-37 utilizing a TFT process sequence deposited on a Silicon substrate, wherein the Gated-FET is constructed using the TFT processing steps. A second process sequence is

disclosed in pages 37-39 utilizing a thinned down SOI substrate, wherein the Gated-FET is constructed in the thinned down SOI portion.

Species II (page 35): The applicant respectfully submits that in page 35, the disclosure details one fabrication embodiment shown in Fig-14 of the Gated-FET. This is a fabrication method to construct the Gated-FET disclosed in Fig-4 and described in pages 14-28. For example, Fig-14.1 illustrates how a thin resistive channel may be formed by depositing a layer of poly silicon, and Fig-14.2 illustrates how this resistive channel may be doped using an implant technique. While Fig-14 is only an illustrative embodiment of the current invention, one skilled in the art may adopt other variations of processing steps to fabricate the Gated-FET device disclosed in Fig-4.

Species III (page 37): The applicant respectfully submits that in page 37, the disclosure details a thinned down SOI fabrication process sequence. This is another fabrication method to construct the Gated-FET disclosed in Fig-4 and pages 14-28. For example, page 38 illustrates how a "Gated-FET mask and Silicon Etch" can be inserted to an SOI process sequence to form a thin resistive channel in the SOI substrate that meets the requirements disclosed in Eqs. 1-17. While the description in page 37-38 is only an illustrative embodiment of the current invention, one skilled in the art may adopt other variations of processing steps to fabricate the Gated-FET device disclosed in Fig-4.

The Applicant respectfully elects Species I on page 13 as the disclosed species in the current application, and lists that all claims 1-20 are readable thereupon. The applicant further submits that the species II and species III identified by the examiner are process variations of fabricating embodiments of the elected Species I.

CONCLUSION

Applicant believes that the above discussion is fully responsive to all grounds of Elections & Restrictions set forth in the Detailed Action.